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Attorney's Docket No. MTI-31271 PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Number: 6,798,259 B2
Issued : September 28, 2004
Patentee : Feng Lin
Title : System and Method to Improve the Efficiency of Synchronous Mirror Delays and Delay Locked Loops

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CERTIFICATION UNDER 37 CFR 1.8(a) and 1.10

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37 CFR 1.8(a) **37 CFR 1.10**

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Transmission

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Date: October 28, 2004 Jon R. Hauch

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ATTENTION: Certificate of Correction Branch

REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT
FOR PTO MISTAKE (37 C.F.R. SECTION 1.322(A))

Sir:

It is requested that a Certificate of Correction be issued correcting printing errors appearing in the above-identified United States Patent.

Attached is Form PTO-1050, with the text of the Certificate in the suggested form suitable for printing.

The column and line number where the errors occur in the issued patent are as follows:

Column 4, line 4: Insert --I/O-- before "system".

Column 6, line 38: Delete "PD" and replace it with --phase detector--.

Column 7, line 40: Replace "din" with --d_{in}--.

Column 8, line 21: Insert --and-- before "adding".

Column 8, line 39: Replace "parameter t_c" with --parameter t_e--.

Column 8, line 48: Replace " parameter t_c" with -- parameter t_e--.

Claim 2, at Column 9, line 28: Replace "arising" with --a rising--.

Claim 8, at Column 9, line 63: After "$t_{mdl} = t_{ck}$;" insert --and--.

Claim 13, at Column 10, line 60: Replace "CDLY signal" with --CDLY signals--.

Claim 14, at Column 10, line 65: Replace "tck" with --t_{ck}--.

Claim 14, at Column 10, line 67: Replace "tmdl" with --t_{mdl}--.

Claim 14, at Column 11, lines 2-4: Delete each occurrence of "wherein".

Claim 18, at Column 11, line 19: Replace "clod" with --clock--.

Claim 18, at Column 11, line 23: Replace "characteristic" with --characteristics--.

Claim 18, at Column 11, line 30: Replace "CIN as t_{mdl}" with --CIN as t_{ck}--.

Claim 19, at Column 11, line 46: Replace "invert" with --inverted--.

Claim 19, at Column 11, line 48: Replace "character" with --characteristics--.

Claim 19, at Column 11, line 61: Replace "CDLY signal" with --CDLY signals--.

Claim 19, at Column 11, line 64: Replace "block" with --clock--.

Claim 23, at Column 12, line 17: Replace "based an" with --based on--.

Claim 25, at Column 12, line 34: Replace "induced" with --reduced--.

Claim 34, at Column 12, line 54: Replace "clack" with --clock--.

Claim 34, at Column 12, line 59: Replace "timing characteristic" with --timing characteristics--.

REMARKS

The errors sought to be corrected in the specification are Patent Office printing errors. Supporting documentation includes the following:

1. A copy of the relevant pages of the Response filed on May 2, 2003, with highlighting of the relevant portions of the amended specification sections; and

2. A copy of the relevant pages of the Supplemental Response filed on April 28, 2004, with highlighting of the relevant portions of the amendments to Claims 2, 8, 13, 14, 18, 19, 26, 28, and 34 (which correspond to issued Claims 2, 8, 13, 14, 18, 19, 23, 25, and 28, respectively).

The requested corrections are to correct printing errors to conform with the specification and claims as allowed by the Examiner during prosecution. Issuance of a Certificate of

Correction would not change either the scope or the meaning of the specification, and re-examination is not required.

As the errors listed are due to the Patent Office's printing mistakes, no fee is necessary in connection with this Certificate.

The Examiner is requested to contact the undersigned Attorney for Applicant should any questions arise with respect to this Request.

Please send the Certificate of Correction to:

Kristine M. Strodthoff
Whyte Hirschboeck Dudek S.C.
555 East Wells Street, Suite 1900
Milwaukee, WI 53202-3819

Dated: October 28, 2004

Kristine M Strodthoff

Kristine M. Strodthoff, Reg. No. 34259
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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,798,259 B2

DATED : September 28, 2004

INVENTOR(S) : Feng Lin

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4, line 4: Insert --I/O-- before "system".
Column 6, line 38: Delete "PD" and replace it with --phase detector--.
Column 7, line 40: Replace "din" with --d_{in}--.
Column 8, line 21: Insert --and-- before "adding".
Column 8, line 39: Replace "parameter t_c" with --parameter t_c--.
Column 8, line 48: Replace " parameter t_c" with -- parameter t_c--.
Claim 2, at Column 9, line 28: Replace "arising" with --a rising--.
Claim 8, at Column 9, line 63: After "$t_{mdl} = t_{ck}$;" insert --and--.
Claim 13, at Column 10, line 60: Replace "CDLY signal" with --CDLY signals--.
Claim 14, at Column 10, line 65: Replace "tck" with --t_{ck}--.
Claim 14, at Column 10, line 67: Replace "tmdl" with --t_{mdl}--.
Claim 14, at Column 11, lines 2-4: Delete each occurrence of "wherein".
Claim 18, at Column 11, line 19: Replace "clod" with --clock--.
Claim 18, at Column 11, line 23: Replace "characteristic" with --characteristics--.
Claim 18, at Column 11, line 30: Replace "CIN as t_{mdl}" with --CIN as t_{ck}--.
Claim 19, at Column 11, line 46: Replace "invert" with --inverted--.
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Claim 34, at Column 12, line 54: Replace "clack" with --clock--.
Claim 34, at Column 12, line 59: Replace "timing characteristic" with --timing characteristics--.

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PATENT NO. 6,798,259

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2004

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

COPY

Application:	09/921,614
Filing Date:	August 3, 2001
Inventors:	Feng Lin
Title:	A Method to Improve the Efficiency of Synchronous Mirror Delays and Delay Locked Loops
Examiner:	Minh T. Nguyen
Art Unit:	2816
Attorney Docket:	MTI-31271 (15225.0027)
Confirmation No.:	7504

CERTIFICATION UNDER 37 CFR 1.8(a) and 1.10

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Date: May 2, 2003 Jill R. Hall

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE

Dear Sir:

Please see the attached.

DOCKET BY JR 5-8-03
CDC BY JR
JHD/Resp. to OA cd 7-2-03 OFF

ATTY INITIALS

NOV 2004

On pages 5-14, please replace the Detailed Description of the Preferred Embodiment with the following:

Referring now to Fig. 1, a system in accordance with the present invention is shown generally by the numeral 10. The system 10 includes a synchronous mirror delay (SMD) circuit 12 and a phase detector control block 14. An external clock signal 16 is input into receiver and buffer 18. This produces clock input signal 20 (CIN), inverted clock input signal (CIN') 21 and clock delay signal 22 (CDLY). Clock delay signal 22 is delayed by an ~~IC~~ I/O system delay t_{mdl} illustrated by block 24. CDLY 22 is also directly fed via line 23 into the SMD 12.

Phase detector control block 14 includes phase detector 26 and associated logical circuitry. The goal of the present invention is to take clock input signal 20 and clock delay signal 22 and, by defining certain characteristics and relationships about the timing of the signals, delineate specific conditions under which the circuit is operating, and direct the signal accordingly. Ultimately, the phase of the signals will determine whether CIN 20 or CIN' 21 is used as the input to the SMD, or whether the SMD is bypassed altogether. Although a specific logic arrangement is shown, it is contemplated that any suitable control logic may be used to define the conditions of the signals and select them accordingly. Associated with the phase detector is a multiplexor 28 which is used as an input selection multiplexor, that is to determine which selection input (CIN or CIN'), based on the difference between CIN signal 20 and CDLY signal 22, to send to the SMD 12. The outputs (collectively 32) of phase detector 26, which will be described in further detail with respect to ~~Fig. 2.~~ Fig. 2 is fed into circuitry control block 30. Circuitry block 30 may be, for instance, a decoder, although any suitable logic is contemplated. The outputs 38 and 40 of phase detection circuitry block 30 will be used to select the outputs for multiplexors 28 and 46, respectively. Based on the signal 38 from control circuitry block 30, input multiplexor 28 will select either CIN 20 or CIN' 21 to be placed on line 48. The output multiplexor 46 is used in combination with the control circuitry block 30 to select which signal is to be put on output line 50. Line 48 (either CIN signal 20 or CIN' signal 21) is directed into the SMD 12. Line 48 is also directed via connection 34 to an input of output selection multiplexor 46. As is known in the art, the SMD 12 includes a measurement delay line composed of a plurality of serially cascaded delay elements (not shown), the measurement delay line having a measurement delay line input and a measurement delay line output. Each delay

Referring now to Fig. 5, the four possible combinations of the logical levels of PH1 signal 32 and PH2 signal 34 are illustrated. Based on the logical levels of each of these signals, ~~such that~~ the condition of the signals may be determined from the logic levels on these lines.

Condition (1):

$$t_{mdl} > t_{ck}/2$$

For condition (1), the effective delay length in the SMD is equal to $t_{ck} - t_{mdl}$. When locking, $t_{lock} = d_{in} + t_{mdl} + (t_{ck} - t_{mdl})$ (measured) + $(t_{ck} - t_{mdl})$ (variable) + $d_{out} = 2t_{ck} + d_{in} + d_{out} - t_{mdl} \approx 2t_{ck}$, where d_{in} and d_{out} are ~~IO~~ I/O intrinsic delays on which t_{mdl} is represented or modeled.

This is the conventional equation to calculate the lock time of the SMD, which is two clock cycles.

Condition (2):

$$t_{mdl} < t_{ck}/2$$

Under this condition, a ~~mux~~ multiplexor is used to select a different phase of CIN to feed in the SMD and the effective delay length is equal to $t_{ck}/2 - t_{mdl}$.

Again, $t_{lock} = d_{in} + t_{mdl} + (t_{ck}/2 - t_{mdl}) + (t_{ck}/2 - t_{mdl}) + d_{out} = t_{ck} + d_{in} + d_{out} - t_{mdl} \approx t_{ck}$.

The lock time is decreased to only one clock cycle. From the previous example,

$$N_{worst} = \frac{15ns/2 - 1ns}{110ps} = 59 \text{ stages}$$

compared to 128 stages without the invention.

Condition (3):

When $t_{mdl} = t_{ck}$, the ~~PD~~ phase detector would declare a lock condition and the clock signal CIN is output directly without even passing into the SMD. The SMD may be disabled to save power.

Condition (4):

are true 85 and decision ~~80D~~ 80d is determined whether t_{mdl} is equal to $t_{ck}/2$. If so ~~82D~~ 82d, condition 4 ~~84D~~ 84d is implicated and it is merely necessary to invert the CIN signal or use an inverted CIN to be input into the clock tree. Again, since there is no need to further delay, the synchronous mirror delay is bypassed and, in a preferred embodiment may be disabled in order to save power. The CIN' signal is input into the clock tree again to distribute the internal clock signal. The result of all four conditions ~~84A-D~~ 84a-d is that lock 86 occurs with an overall reduction in delay stages, which is the purpose of the circuit while maintaining the desired operating range.

Referring now to Fig. 7, the present invention is shown being used in a delay-locked loop or DLL, which is shown generally by the numeral 200. An external clock signal 216 is input into receiver and buffer 218. This produces clock input signal (CIN) 220. The delay in the signal as it passes through buffer receiver 218 is represented by d_{in} 219. CIN signal 220 is input via branch 222 into phase detector 226. CIN signal 220 is also directed via branch 224 into delay line 228. Phase detector 226 may include any associated logical circuitry. The goal of the present invention is to take CIN signal 220 as well as a clock feedback signal 230 (CKFB) and, by defining particular characteristics and relationships about the timing of CIN signal 220 and CKFB 230, to delineate specific conditions under which the signals are operating, and selecting and directing the signals accordingly. Although a specific logic arrangement is shown, it is contemplated that any suitable control logic may be used to define the conditions of the signals and then selecting them accordingly. CKFB feedback signal 230 is a typical feedback loop as is found in a common delayed-lock loop (DLL). Phase detector 226 compares the timing of signal CIN and signal CKFB. Based on timing conditions and characteristics of each signal, control signals are sent via control lines 232 to control block 234 and output via lines 236 to delay line 228. The period of the delay is represented by t_{delay} 230. Associated with the delay line 228 is selector 238 which receives an input 240 from the phase detector 226 as well as inputs 242 and 244 representative of the clock CLK and inverted clock signals respectively. Selector 238 selects, based on the input 240 from the phase detector 226, whether to put signal 242 or 244 to input 246 into clock tree driver 248. The period of delay by the driver is represented by t_{tree} 250. The output 252 of the clock tree driver 248 is sent to an output buffer 254 which has an input data line 256 and a data output line 258. The delay by the output of data is represented by the parameter d_{out} 260. Clock tree driver 248, as part of the delay-locked loop, feeds back into phase

detector 226 via line 230. The delay associated with the ~~IO~~ I/O model 262 is represented by the parameter d_{in} and d_{out}.

Generally speaking,

1. In order to synchronize XCLK with DQs,

$t_{delay} = t_{ck} - t_{tree} - (d_{in} + d_{out})$

In traditional DLLs, the delay stages required are:

$$N = \frac{t_{delay}}{t_d} = \frac{t_{ck} - t_{tree} - (d_{in} + d_{out})}{t_d}$$

$$N_{worst} = \frac{t_{ck}\,(long) \quad - \quad t_{tree}\,(short) - (d_{in} + d_{out})\,(fast)}{t_d\,(fast)}$$

$$= \frac{15n - 1n}{110\ ps} \approx 128$$

2. Use the same method and adding a selector:

$t_e < t_{ck}/2$, $t_{delay} = t_{ck}/2 - t_e$

$t_e > t_{ck}/2$, $t_{delay} = t_{ck} - t_e$

For both cases,

t_{delay} is less than or equal to $t_{ck}/2$

$$N_{worst} = \frac{t_{ck}/2\,(long) - others}{t_d\,(fast)} = \frac{7.5n - 1n}{110\ ps} \approx 59$$

Referring now to Fig. 8, a timing diagram for signals CIN and CKFB are shown in a particular arrangement. The period from the rising edge 300 to rising edge 302 is designated as t_{ck}. The amount of time from rising edge 300 of CIN and rising edge 304 of CKFB is represented by the parameter t_e. Additionally, the parameter from the rising edge 304 of CKFB and the falling edge 306 of CIN is represented by the parameter t_{delay}. In this case, t_{delay} is less than or equal to half of t_{ck}.

Referring now to Fig. 9, the second case is illustrated where CKFB does not fire until after the first pulse of CIN. Again, ~~t_{ck} is~~ t_{ck} is represented by the rising edge 308 of CIN and the next rising edge 310 of CIN. Additionally, the length of time from the rising edge 308 to the rising edge 312 of CKFB is shown by the parameter t_c. However, in this instance, ~~t_{delay} is~~ t_{delay} is measured from the rising edge 312 of CKFB until the next rising edge 310 of CIN. Similarly, in this case, ~~t_{delay} is~~ t_{delay} is less than or equal to one-half of the clock period t_{ck}.

Fig. 10 is a block diagram of a computer system 100. The computer system 100 utilizes a memory controller 102 in communication with SDRAMs 104 through a bus 105. The memory controller 102 is also in communication with a processor 106 through a bus 107. The processor 106 can perform a plurality of functions based on information and data stored in the SDRAMs 104. One or more input devices 108, such as a keypad or a mouse, are connected to the processor 106 to allow an operator to manually input data, instructions, etc. One or more output devices 110 are provided to display or otherwise output data generated by the processor 106. Examples of output devices include printers and video display units. One or more data storage devices 112 may be coupled to the processor 106 to store data on, or retrieve information from, external storage media. Examples of storage devices 112 and storage media include drives that accept hard and floppy disks, tape cassettes, and CD read only memories.

While the present invention has been described in conjunction with preferred embodiments thereof, many modifications and variations will be apparent to those of ordinary skill in the art. For example, although the present invention is directed to synchronous mirror delay systems, the present invention is contemplated to be used with any implementable logic devices and in other arrangements, such as in a digital delay locked loop (DDLL), to improve the efficiency in that arrangement. The foregoing description and the following claims are intended to cover all such modifications and variations.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application:	09/921,614
Filing Date:	August 3, 2001
Inventor:	Feng Lin
Title:	A Method to Improve the Efficiency of Synchronous Mirror Delays and Delay Locked Loops
Examiner:	Minh T. Nguyen
Art Unit:	2816
Attorney Docket:	MTI-31271 (15225.0027)
Confirmation No.:	7504
Customer No.:	31870

CERTIFICATION UNDER 37 CFR 1.8(a) and 1.10

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37 CFR 1.8(a) **37 CFR 1.10**

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Transmission

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Date: April 28, 2004 Bernadette M. Jackson

Commissioner for Patents
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Alexandria, VA 22313-1450

SUPPLEMENTAL RESPONSE

Dear Sir:

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ATTY INITIALS _____

AMENDED CLAIMS

1. (previously presented) A method of improving the efficiency of synchronizing a clock signal for an integrated circuit, comprising:

providing a clock input signal (CIN), an inverted clock input signal (CIN'), and a clock delay signal (CDLY);

detecting a plurality of phases of CIN and CDLY based on timing conditions associated with CIN and CDLY; and

selectively inputting CIN or CIN' into a synchronous mirror delay (SMD) based on the phase of CIN and CDLY to reduce a number of delay stages in the SMD.

Claim 2

2. (previously presented) The method of claim 1 wherein the timing conditions include a period of CIN (t_{ck}) and a period from a rising edge in CIN to a rising edge in CDLY (t_{mdl}), and selectively inputting includes inputting CIN into the SMD when $t_{mdl} > t_{ck}/2$ and inputting CIN' into the SMD when $t_{mdl} < t_{ck}/2$ to reduce the number of delay stages in the SMD.

3. (original) The method of claim 2 wherein the number of delay stages in the SMD is reduced substantially in half.

4. (previously presented) The method of claim 2 wherein the SMD has a plurality of delay lines, and the number of delay stages in at least one of the SMD delay lines is reduced substantially to 59 from 128.

Claim 8

8. (previously presented) The method of claim 5 further including defining the timing characteristics as a period of CIN as t_{ck} and defining a period from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and wherein determining includes determining that the phases include:

a first phase when $t_{mdl} > t_{ck}/2$;

a second phase when $t_{mdl} < t_{ck}/2$;

a third phase when $t_{mdl} = t_{ck}$; and

a fourth phase when $t_{mdl} = t_{ck}/2$.

9. (previously presented) A method of synchronizing a clock signal for an integrated circuit, comprising:

providing an internal clock signal (CIN), an inverted internal clock signal (CIN'), and a clock delay signal (CDLY) having timing characteristics;

differentiating, with a phase detector, a plurality of phases based upon the timing characteristics of CIN and CDLY; and

selecting, based on the phases, one of CIN and CIN' to be input into a synchronous mirror delay (SMD) thereby reducing a number of delay stages in the SMD.

Claim 13

13. (currently amended) ~~A memory device, comprising:~~

~~a synchronous mirror delay (SMD); and~~

~~a phase detector in electronic communication with the SMD and comprising:~~

~~means for receiving a clock input signal (CIN) and a clock delay signal (CDLY), the CIN and CDLY each having timing characteristics; and~~

~~means for outputting a pair of branches each having a logical level, the logical levels of the branches defining a plurality of conditions based on the timing characteristics of CIN and CDLY;~~

~~wherein for at least one of the plurality of conditions, the memory device comprises means for reducing a number of delay stages for a selected signal to pass through the SMD based on one of the plurality of conditions~~.

A memory device, comprising:

a synchronous mirror delay (SMD); and

a phase detector control block in electronic communication with the SMD, wherein the phase detector control block receives a clock input signal (CIN), an inverted clock input signal (CIN'), and a clock delay signal (CDLY), the CIN and CDLY signals each having timing characteristics, the phase detector control block detects a plurality of conditions based on the timing characteristics of the CIN and CDLY signals, and outputs a selected signal selected between the CIN and CIN' signals and the CDLY signal to the SMD, the timing characteristics of the CIN and CDLY signals are used to select the selected signal to the SMD to reduce a number of delay stages in the SMD for the selected signal passing through.

Claim 14

14. (previously presented) The memory device of claim 13 wherein the timing characteristics include a period of CIN defined as t_{ck} and a rising edge from CIN to a rising edge in CDLY is defined as t_{mdl}; and

a first phase is when $t_{mdl} > t_{ck}/2$;

a second phase is when $t_{mdl} < t_{ck}/2$;

a third phase is when $t_{mdl} = t_{ck}$; and

a fourth phase is when $t_{mdl} = t_{ck}/2$.

15. (previously presented) The memory device of claim 14 wherein when $t_{mdl} < t_{ck}/2$ the number of delay stages in the SMD is comparable to when $t_{mdl} > t_{ck}/2$.

16. (previously presented) The memory device of claim 14 wherein the number of delay stages when $t_{mdl} < t_{ck}/2$ is reduced by substantially one-half.

17. (previously presented) The memory device of claim 14 wherein the number of delay stages when $t_{mdl} < t_{ck}/2$ is reduced from 128 to substantially 59.

Claim 18

18. (currently amended) ~~A synchronous mirror delay system, comprising:~~

~~a synchronous mirror delay (SMD); and~~

~~a phase detector in electronic communication with the SMD and comprising:~~

~~means for receiving a clock input signal (CIN) and a clock delay signal (CDLY), the CIN and CDLY each having timing characteristics; and~~

~~means for outputting a pair of branches each having a logical level, the logical levels of the branches defining a plurality of conditions based on the timing characteristics of CIN and CDLY~~

~~wherein for at least one of the plurality of conditions, the system comprises means for reducing a number of delay stages for a selected signal to pass through the SMD based on one of the plurality of conditions, the timing characteristics define a period of CIN as t_{ck} and also define a period from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and the plurality of conditions include:~~

~~a first phase when $t_{mdl} > t_{ck}/2$;~~

~~a second phase when $t_{mdl} < t_{ck}/2$;~~

~~a third phase when $t_{mdl} = t_{ck}$; and~~

~~a fourth phase when $t_{mdl} = t_{ck}/2$;~~

~~means for reducing the number of delay stages in the second; and~~

~~means for CIN to bypass the SMD in the third and fourth phases.~~

A synchronous mirror delay system, comprising:

a synchronous mirror delay (SMD); and

a phase detector control block in electronic communication with the SMD, wherein the phase detector control block receives a clock input signal (CIN), an

Claim 18 cont.

inverted clock input signal (CIN'), and a clock delay signal (CDLY), the CIN and CDLY signals each having timing characteristics, the phase detector control block detects a plurality of conditions based on the timing characteristics of the CIN and CDLY signals, and outputs a selected signal selected between the CIN and CIN' signals and the CDLY signal to the SMD, the timing characteristics of the CIN and CDLY signals are used to select the selected signal to the SMD to reduce a number of delay stages in the SMD for the selected signal passing through, the timing characteristics define a period of CIN as t_{ck} and also define a period from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and the plurality of conditions include:

a first phase when $t_{mdl} > t_{ck}/2$;

a second phase when $t_{mdl} < t_{ck}/2$;

a third phase when $t_{mdl} = t_{ck}$; and

a fourth phase when $t_{mdl} = t_{ck}/2$;

wherein the phase detector control block selects the selected signal such that the number of delay stages in the second phase is reduced and the selected signal is the CIN signal bypassing the SMD in the third and fourth phases.

Claim 19

19. (currently amended) ~~A synchronizing circuit for use with an integrated circuit, comprising:~~

~~an input buffer comprising means for receiving an external clock signal to produce a clock input signal (CIN), an inverted clock input signal (CIN'), and a clock delay signal (CDLY), each having timing characteristics;~~

~~a synchronous mirror delay (SMD) having a measurement delay line input for connection to a measurement delay line, a measurement delay line output connected to a variable delay line input for connection to a variable delay line, the variable delay line including a variable delay line output; and~~

~~a phase detector disposed between the input buffer and the SMD, the phase detector having a first input means for receiving the CIN, a second input means for receiving the CDL, means for generating one of a plurality of output signal combinations, each combination corresponding to a phase of the CIN and CDLY signals based on the timing characteristics, means for connecting a CDLY SMD input to the measurement delay line input, means for connecting a SMD output connected to the variable delay line output, and a circuit selectively inputting CIN or CIN' as a CIN SMD input based on the phase of the signals, wherein for at least one of the phases, a number of delay stages is reduced for the external clock signal to pass through the SMD.~~

A synchronizing circuit for use with an integrated circuit, comprising:

an input buffer for receiving an external clock signal to produce a clock input signal (CIN), an inverted clock input signal (CIN'), and a clock delay signal (CDLY), each having timing characteristics;

a synchronous mirror delay (SMD) having a measurement delay line input, a variable delay line input, and a variable delay line output; and

a phase detector control block disposed between the input buffer and the SMD, the phase detector having a first input for receiving the CIN, a second input for receiving the CDLY and a third input for receiving the CIN', wherein the phase detector control block detects a plurality of conditions based on the timing characteristics of the CIN and CDLY signals, and outputs a selected signal selected between the CIN and CIN' signals to the variable delay line input and the CDLY signal to the measurement delay line input, the timing characteristics of the CIN and CDLY signals are used to select the selected signal to the variable delay line input to reduce a number of delay stages in the SMD for the external clock signal passing through.

20. (previously presented) The circuit of claim 19 wherein the timing characteristics define a period of CIN as t_{ck} and also define a period from a rising edge in CIN to a rising edge in CDLY as t_{mdl}, and when $t_{mdl} < t_{ck}/2$, CIN' is input into the SMD and when $t_{mdl} > t_{ck}/2$ CIN is input into the SMD.

21. (previously presented) The circuit of claim 20 wherein the number of delay stages in the SMD when $t_{mdl} < t_{ck}/2$ is reduced.

22. (previously presented) The circuit of claim 20 wherein the number of delay stages in the SMD when $t_{mdl} < t_{ck}/2$ is reduced from 128 to substantially 59.

23-25. (canceled)

Claim 23

26. (currently amended) ~~A system, comprising:~~

~~a phase detector comprising means for receiving a clock input signal (CIN) and a clock delay signal (CDLY), each signal having timing conditions, and means for generating a plurality of output signal combinations, each combination based upon the timing conditions; and~~

~~logic in electronic communication with the phase detector to select one of the output signal combinations corresponding to the timing conditions of the signals;~~

~~wherein the system selectively feeds CIN or an inverted clock input signal (CIN') into a synchronous mirror delay ("SMD") based upon the plurality of output signal combinations to reduce a number of delay stages for a selected signal to pass through the SMD.~~

A system, comprising:

a synchronous mirror delay (SMD); and

a phase detector control block in electronic communication with the SMD, wherein the phase detector control block comprises a phase detector, a logic circuit, and multiplexers, wherein the phase detector control block receives a clock input signal (CIN), an inverted clock input signal (CIN'), and a clock delay signal (CDLY), the CIN and CDLY signals each having timing characteristics, the phase detector control block detects a plurality of conditions based on the timing characteristics of the CIN and CDLY signals, and outputs a selected signal selected between the CIN and CIN' signals and the CDLY signal to the SMD, the timing characteristics of the CIN and CDLY signals are used to select the selected signal to the SMD to reduce a number of delay stages in the SMD for the selected signal passing through.

27. (previously presented) The system of claim 26 wherein the timing characteristics include a period of CIN defined as t_{ck} and a rising edge from CIN to a rising edge in CDLY is defined as t_{mdl}; and the phases include:

a first phase when $t_{mdl} > t_{ck}/2$;

a second phase when $t_{mdl} < t_{ck}/2$;

a third phase when $t_{mdl} = t_{ck}$; and

a fourth phase when $t_{mdl} = t_{ck}/2$.

Claim 25

28. (previously presented) The system of claim 27 wherein the number of delay stages is reduced.

29. (previously presented) The system of claim 27 wherein the number of delay stages is reduced substantially by one-half.

30. (previously presented) The system of claim 27 wherein the number of delay stages in the SMD when $t_{mdl} < t_{ck}/2$ is reduced from 128 to substantially 59.

31-33. (canceled)

Claim 28

34. (currently amended) ~~A system, comprising:~~

~~a processor;~~

~~a memory controller;~~

~~a plurality of memory devices;~~

~~a first bus interconnecting the processor and memory controller;~~

~~a second bus interconnecting the memory controller and the plurality of memory devices;~~

~~each of the memory devices having:~~

~~a synchronous mirror delay (SMD);~~

~~a phase detector comprising means for receiving a clock input signal (CIN) and a clock delay signal (CDLY), each signal having timing conditions including a period of CIN (t_{ck}) and a period from a rising edge in CIN to a rising edge in CDLY (t_{mdl}); and means for generating a plurality of output signal combinations, each combination corresponding to phases of the signals based upon the timing conditions; and~~

~~logic in electronic communication with the phase detector to select one of the output signal combinations corresponding to the timing conditions of the signals to input CIN into the SMD when $t_{mdl} > t_{ck}/2$ and input CIN' into the SMD when $t_{mdl} < t_{ck}/2$ to reduce a number of delay stages in the SMD.~~

A system, comprising:

processor;

a memory controller;

a plurality of memory devices;

a first bus interconnecting the processor and memory controller;

Claim 28 cont.

a second bus interconnecting the memory controller and the plurality of memory devices;

each of the memory devices having:

a synchronous mirror delay (SMD); and

a phase detector control block in electronic communication with the SMD, wherein the phase detector control block comprises a phase detector, a logic circuit, and multiplexers, wherein the phase detector control block receives a clock input signal (CIN), an inverted clock input signal (CIN'), and a clock delay signal (CDLY), the CIN and CDLY signals each having timing characteristics, the phase detector control block detects a plurality of conditions based on the timing characteristics of the CIN and CDLY signals, and outputs a selected signal selected between the CIN and CIN' signals and the CDLY signal to the SMD, the timing characteristics of the CIN and CDLY signals are used to select the selected signal to the SMD to reduce a number of delay stages in the SMD for the selected signal passing through.

35-81. (canceled)